output signals for application to speakers 152, 154. It should be noted that the exemplary systems illustrated in FIG. 1 may be configured to introduce delay between the various multiple bit streams, in order to provide additional time diversity.--

Please replace the paragraph beginning at page 8, line 19 with the following rewritten paragraph:

--FIG. 4 shows a portion of a transmitter 250 which represents an alternative implementation of the transmitter 200 of FIG. 3. The transmitter 250 includes an audio processor 252, a channel stream processor 256, and a set of hardware 254 which implements the IF interface 206 and the global timing process 230. In the audio processor 252, an analog audio source is applied to A/D converter 212, and multiplexed with a digital audio source in a multiplexer 259. An output of the multiplexer 259 is applied to the above-described multi-stream PAC encoder 215, and the multi-stream output of the PAC encoder 215 is partially encrypted in the encryption device 210 in the manner previously described. The encryption device 210 in this embodiment is assumed to be part of the audio processor 252. The output of the encryption device is applied to an ancillary data combiner 262, and combined with data from an ancillary data source, if any. Different delays may be applied to one or more of the multiple bitstreams in a staggered stream delay (SSD) element 264, in order to provide the above-noted time diversity between the bitstreams.--

Please replace the paragraph beginning at page 9, line 3 with the following rewritten paragraph:

--The channel stream processor 256, which may be implemented in whole or in part in software, includes an auxiliary data combiner 266 which receives the multiple bitstreams from the SSD element 264. The auxiliary data combiner 266 combines the multiple streams with auxiliary data from an auxiliary data source and service data 272, as delivered from a data multiplexer 274 and data encoder 276. Data encoder 276 may be, e.g., a Reed-Solomon (RS) encoder. An interface control element 270 interacts with the global timing process 230 to handle the transfer of control and

a2

monitor information between the channel stream processor 256 and, e.g., other portions of the transmitter or other system devices.--

Please replace the paragraph beginning at page 10, line 16 with the following rewritten paragraph:

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--One or more of the service processes 310, as well as other elements of the receiver 300, may be implemented at least in part using a digital signal processor, an ASIC, an FPGA, as well as portions or combinations of these and other types of processors. For example, the decryption device 325, the PAC audio decoder 326, the data decoder 327, and an interface to the recording device 328, may be implemented at least in part using a DSP, while the SEP 318, OFDM/DQPSK demodulator 320, error correction layers 322, and PH 335, may be implemented in a combination of an ASIC and an FPGA. More particularly, implementing the decryption device 325 and recording device interface as DSP code in a read-only memory (ROM) of a DSP ensures that these elements will be less susceptible to unauthorized access after manufacture.--

Please replace the paragraph beginning at page 14, line 16 with the following rewritten paragraph:

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--FIG. 7 illustrates examples of the manner in which a given recorded audio selection may be played back. A given recorded encrypted selection 420 may be played back for a designated period of time, e.g., 30 days, at a reduced quality level prior to purchase. This allows the user ample time to decide whether to purchase the recorded audio selection or to discard it. The recorded encrypted selection may be read in operation 424, which discards the encrypted streams and checks the corresponding expiration date. The selection is then applied to a single-stream PAC decoder 430 for playback through an audio output system 430 at, e.g., an FM-quality level.--